# Microtronix HDMI 1.4 Receiver HSMC Daughter Card

USER MANUAL REVISION 1.0





# Document Revision History

This user guide provides basic information about using the **Microtronix HDMI 1.4 Receiver HSMC Daughter Card, (PN: 6291-01-01)**. The following table shows the document revision history.

Date	Rev	Description
Feb. 2013	1.0	Release
Jan. 2013	0.9	Beta release

## **How to Contact Microtronix**

#### E-mail

Sales Information: sales@microtronix.com

Support Information: support@microtronix.com

#### Website

Software updates to the **HDMI 1.4 Receiver HSMC Daughter Card** and supporting Microtronix IP Cores are listed on the download page of our website and made available via an email request form. Some product upgrades are only available to customers who have purchased the ViClaro III or ViClaro IV-GX Development kit.

The upload site is for sending files to Technical Support.

General Website: http://www.microtronix.com

Downloads Page: http://www.microtronix.com/downloads/

FTP Upload Site: http://microtronix.leapfile.com

#### **Phone Numbers**

General: (001) 519-690-0091

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## **Typographic Conventions**

Path/Filename	A path/filename
[SOPC Builder]\$ <cmd></cmd>	A command that should be run from within the Cygwin Environment.
Code	Sample code.
-	Indicates that there is no break between the current line and the next line.

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#### Introduction

The Microtronix *HDMI 1.4 Receiver HSMC Daughter Card* is targeted at the development of 12-bit Deep Color HD video systems. It is designed to interface an HDMI Receiver to an Altera FPGA Development Kit using the HSMC expansion connector.

The key features of the board include:

- Analog Devices ADV7612 HDMI 1.4 Receiver Interface
  - o HDMI v1.4 Receiver
  - o 12-bit Deep Color
  - o 3D video ready
  - o Supports RGB, YCbCr and DDR video
- · Quartus Reference Design
- Altera compatible HSMC expansion connector

#### **Kit Contents**

The Microtronix *HDMI 1.4 Receiver HSMC Daughter Card* is includes the following hardware components:

- HDMI 1.4 Receiver HSMC Daughter Card (PN: 6290-01-01)
  - o Card mounting hardware
- Installation CD

**NOTE:** The CD is not supplied when the HDMI card is purchased in conjunction with a Microtronix ViClaro III or ViClaro IV-GX Development Kit.

#### **Board Overview**

The Microtronix *HDMI 1.4 Receiver HSMC Daughter Card* uses the Analog Device ADV7612BSWZ-P high-performance HDMI v1.4 Receiver to support HDTV formats up to 1080p at 60 Hz. using a 225 MHz, high-definition multimedia interface (HDMI 1.4) transmitter.

A picture of the card is shown below.



Figure 1: HDMI 1.4 Receiver HSMC Daughter Card

#### **Power Supply**

The card operates from 3.3 VDC supplied from the HSMC connector.

#### **Power Consumption**

The HDMI Transmitter board draws approximately 1A at 3.3 VDC. Power consumption varies according to the transmit video resolution.

#### **HDMI 1.4 Receiver Card Components**

The Microtronix *HDMI 1.4 Receiver HSMC Daughter Card* incorporates the following components and devices:

- Analog Devices ADV7612 HDMI v1.4 Receiver Interface
- Misc:
  - TSV voltage clamps

For more information on the IC components, contact the respective vendors.

## Introduction to HDMI Interfaces

The **High-Definition Multimedia Interface (HDMI)** is a compact connector interface for transmitting uncompressed digital video/audio streams. It is widely used across a broad range of consumer devices including: set-top TV boxes, Blu-ray Disk players, personal computers, televisions, and AV receivers.

The interface uses a Transition Minimized Differential Signaling (TMDS)-based protocol and electrical signaling

The HDMI cable and connectors carry four differential pairs that make up the TMDS data and clock channels. These channels are used to carry video, audio and auxiliary data. In addition, HDMI carries a VESA DDC channel. The DDC is used for configuration and status exchange between a single Source and a single Sink. The optional CEC protocol provides high-level control functions between all of the various audiovisual products. This feature is not supported by reference design.

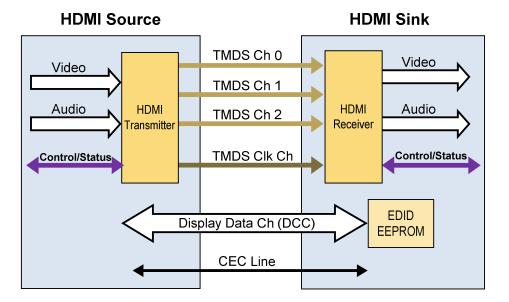


Figure 2: HDMI System Architecture

#### **EDID Interface**

Extended display identification data (EDID) is a data structure provided by a display panel to describe its capabilities to a graphics card. EDID is defined by a standard published by the Video Electronics Standards Association (VESA). The EDID includes manufacturer name, product type, phosphor or filter type, timings supported by the display, display size, luminance data and (for digital displays only) pixel mapping data.

EDID functionality is supported on the HSMC HDMI card.

#### **HDMI Connector Pin Assignments**

The card incorporates a Type A connector which has 19 pins. The pin assignment is shown in the following table.

**Table 1: HDMI Type A Connector Pin Assignment** 

Pin	Signal Name	Pin	Signal Name
1	TMDS Data2+	2	TMDS Data2 Shield
3	TMDS Data2+	4	TMDS Data1+
5	TMDS Data1 Shield	6	TMDS Data1+
7	TMDS Data0+	8	TMDS Data0 Shield
9	TMDS Data0+	10	TMDS Clock+
11	TMDS Clock Shield	12	TMDS Clock-
13	CEC	14	Reserved (N.C.)
15	SCL	16	SDA
17	DDC/CEC Ground	18	+5V Power
19	Hot Plug Detect		

#### I<sup>2</sup>C 2-Wire Serial Bus

The HDMI Transmitter card used an I<sup>2</sup>C Bus to configure the ADV7511 video transmitter. The I2C SDA and SCL bus signals are connected to the assigned pins (33 & 34) of the HSMC connector. The user can access I<sup>2</sup>C connected devices from a Host board using a Microtronix I<sup>2</sup>C Master IP Core programmed into the FPGA device.

Table 2: I<sup>2</sup>C Addresses

Device	I <sup>2</sup> C Address
ADV7612	0x98

## **HDMI Receiver J1**

The HDMI 1.4 Receiver HSMC Connector, J1 interfaces the HDMI 1.4 **HSMC Connector**, **Receiver HSMC Daughter Card** to the Host FPGA Development board.

> The J1 pin assignments in Table 3 below show the Cyclone III FPGA pin mapping when the HDMI 1.4 Receiver board is installed on HSMC Header J4, (the LVDS header) of the ViClaro III Board.

Table 3: ViClaro III FPGA – HDMI 1.4 Receiver board HSMC Connector Pin **Assignment Mappings** 

Cyclone III Pin #	Signal Name	HSMC Pin #	HSMC Pin#	Signal Name	Cyclone III Pin #
	NC	1	2	NC	
	NC	3	4	NC	
	NC	5	6	NC	

	NC	7	8	NC	
AE3	NC	9	10	NC	AE2
AF2	NC	11	12	NC	AE1
AC3	NC	13	14	NC	AD2
AD3	NC	15	16	NC	AD1
AC5	NC	17	18	NC	AC2
AC4	NC	19	20	NC	AC1
AB6	NC	21	22	NC	AB2
AB5	NC	23	24	NC	AB1
AA6	NC	25	26	NC	AA4
AA5	NC	27	28	NC	AA3
Y6	NC	29	30	NC	Y4
Y5	NC	31	32	NC	Y3
Y10	I2C_SDA	33	34	I2C_SCL	AA10
	NC	35	36	NC	
	NC	37	38	NC	
	NC	39	40	NC	
Т8	VIDEO_P35	41	42	VIDEO_P34	Т7
M5	VIDEO_P33	43	44	VIDEO_P32	L5
	3.3V	45	46	12V	
W8	VIDEO_P31	47	48	VIDEO_P30	W2
Y7	VIDEO_P29	49	50	VIDEO_P28	W1
	3.3V	51	52	12V	
V8	VIDEO_P27	53	54	VIDEO_P26	W4
V7	VIDEO_P25	55	56	VIDEO_P24	W3
	3.3V	57	58	12V	
V6	VIDEO_LLO	59	60	VIDEO_P23	V4
V5	VIDEO_P22	61	62	VIDEO_P21	V3
	3.3V	63	64	12V	
U6	VIDEO_P20	65	66	VIDEO_P19	V2
U5	VIDEO_P18	67	68	VIDEO_P17	V1
	3.3V	69	70	12V	
R7	VIDEO_P16	71	72	VIDEO_P15	U2
R6	VIDEO_P14	73	74	VIDEO_P13	U1
	3.3V	75	76	12V	

M8	VIDEO_P12	77	78	VIDEO_P11	U3
M7	VIDEO_P10	79	80	VIDEO_P9	U4
	3.3V	81	82	12V	
K8	VIDEO_P8	83	84	VIDEO_P7	T4
L8	VIDEO_P6	85	86	VIDEO_P5	Т3
	3.3V	87	88	12V	
J7	VIDEO_P4	89	90	VIDEO_P3	R2
K7	VIDEO_P2	91	92	VIDEO_P1	R1
	3.3V	93	94	12V	
R3	VIDEO_D0	95	96	VIDEO_DE	Y2
R4	VIDEO_HS	97	98	VIDEO_VS_FIELD	Y1
	3.3V	99	100	12V	
M4	AUDIO_AP0	101	102	AUDIO_DSD1	L4
M3	AUDIO_AP2	103	104	AUDIO_DSD3	L3
	3.3V	105	106	12V	
P2	AUDIO_AP4	107	108	AUDIO_SCLK_INT2	L2
P1	AUDIO_AP5	109	110	AUDIO_MCLK_INT2F	L1
	3.3V	111	112	12V	
N4	INT1	113	114	RESETn	K4
N3		115	116	CSn	K3
	3.3V	117	118	12V	
L7		119	120		K2
L6		121	122		K1
	3.3V	123	124	12V	
J6		125	126		J4
J5		127	128		J3
	3.3V	129	130	12V	
M2		131	132		H4
M1		133	134		H3
	3.3V	135	136	12V	
G6		137	138		G2
G5		139	140		G1
	3.3V	141	142	12V	
G4		143	144		F2
G3		145	146		F1
	I				

	3.3V	147	148	12V	
D2		149	150		E3
D1		151	152		F3
	3.3V	153	154	12V	
D3		155	156		J2
C2		157	158		J1
	3.3V	159	160	Presence LED	

The pin assignments of Table 4 below apply when the HDMI 1.4 Receiver board is installed on the ViClaro IV-GX Host board using HSMC Header J1.

Table 4: ViClaro IV-GX FPGA – HDMI 1.4 Receiver board HSMC Connector Pin Assignment Mappings

Cyclone IV Pin #	Signal Name	HSMC Pin #	HSMC Pin #	Signal Name	Cyclone IV Pin #
	NC	1	2	NC	
	NC	3	4	NC	
	NC	5	6	NC	
	NC	7	8	NC	
	NC	9	10	NC	
	NC	11	12	NC	
	NC	13	14	NC	
	NC	15	16	NC	
AB4	NC	17	18	NC	AC2
AB3	NC	19	20	NC	AC1
Y4	NC	21	22	NC	AA2
Y3	NC	23	24	NC	AA1
V4	NC	25	26	NC	W2
V3	NC	27	28	NC	W1
T4	NC	29	30	NC	U2
Т3	NC	31	32	NC	U1
J9	I2C_SDA	33	34	I2C_SCL	H9
	NC	35	36	NC	

		1	1		1
	NC	37	38	NC	
G6	NC	39	40	NC	L11
F17	VIDEO_P35	41	42	VIDEO_P34	G14
F16	VIDEO_P33	43	44	VIDEO_P32	G15
	3.3V	45	46	12V	
E15	VIDEO_P31	47	48	VIDEO_P30	G12
D14	VIDEO_P29	49	50	VIDEO_P28	G13
	3.3V	51	52	12V	
D13	VIDEO_P27	53	54	VIDEO_P26	G10
D12	VIDEO_P25	55	56	VIDEO_P24	F11
	3.3V	57	58	12V	
D11	VIDEO_LLO	59	60	VIDEO_P23	F8
E10	VIDEO_P22	61	62	VIDEO_P21	F9
	3.3V	63	64	12V	
E9	VIDEO_P20	65	66	VIDEO_P19	F6
D8	VIDEO_P18	67	68	VIDEO_P17	G7
	3.3V	69	70	12V	
E7	VIDEO_P16	71	72	VIDEO_P15	F4
E6	VIDEO_P14	73	74	VIDEO_P13	F5
	3.3V	75	76	12V	
D5	VIDEO_P12	77	78	VIDEO_P11	F10
E4	VIDEO_P10	79	80	VIDEO_P9	F7
	3.3V	81	82	12V	
E3	VIDEO_P8	83	84	VIDEO_P7	C2
D3	VIDEO_P6	85	86	VIDEO_P5	D4
	3.3V	87	88	12V	
D1	VIDEO_P4	89	90	VIDEO_P3	C4
E16	VIDEO_P2	91	92	VIDEO_P1	C3
	3.3V	93	94	12V	
D16	VIDEO_D0	95	96	VIDEO_DE	D6
C16	VIDEO_HS	97	98	VIDEO_VS_FIELD	C5
	3.3V	99	100	12V	
A4	AUDIO_AP0	101	102	AUDIO_DSD1	C7
A5	AUDIO_AP2	103	104	AUDIO_DSD3	D7
	3.3V	105	106	12V	
	ı			1	1

A6	AUDIO_AP4	107	108	AUDIO_SCLK_INT2	D10
A7	AUDIO_AP5	109	110	AUDIO_MCLK_INT2F	D9
	3.3V	111	112	12V	
A8	INT1	113	114	RESETn	C12
A9		115	116	CSn	C11
	3.3V	117	118	12V	
A10		119	120		C14
A11		121	122		F14
	3.3V	123	124	12V	
A12		125	126		C15
A13		127	128		D15
	3.3V	129	130	12V	
A14		131	132		F13
B16		133	134		F15
	3.3V	135	136	12V	
A16		137	138		E12
D17		139	140		F12
	3.3V	141	142	12V	
A17		143	144		E13
C17		145	146		C6
	3.3V	147	148	12V	
C9		149	150		B6
В9		151	152		B7
	3.3V	153	154	12V	
B10		155	156		C13
C10	HSMC1_D78	157	158	HSMC1_D79	B12
	3.3V	159	160	Presence LED*	

<sup>\*</sup> Note: Connect to GND to turn LED on.

# Software Installation

NOTE: This section only applies if the HDMI 1.4 Receiver HSMC Daughter Card was purchased as a stand-alone board. When the card is purchased in conjunction with the Microtronix ViClaro III or ViClaro IV-GX HD Video IP Development Kit, the HDMI reference designs are supplied as part of the ViClaro III or ViClaro IV-GX Software Installation CD.

The HDMI 1.4 Receiver Card software may also be supplied by Microtronix on a CD or via FTP as a zipped file. If you received the latter, unzip the file to a temporary file directory and run the setup.exe file. The software should self-install from the CD or it can be manually installed by running the setup.exe file.

WARNING: Remove older installations of the HDMI 1.4 Receiver Card software from the PC prior to installing the new version of software.

## 1.4 Receiver Reference **Designs**

Overview of HDMI The HDMI 1.4 Receiver board is supplied with a basic reference design for; the Microtronix ViClaro III (Cyclone III), the ViClaro IV-GX (Cyclone IV-GX) and for the Terrasic DE4 (Stratix IV) Development Kits. It includes a pre-compiled SOF file and the Quartus II 12.1 project files.

> The receiver design requires the use of the Microtronix HDMI 1.4 Transmitter board to loop or pass video between the HDMI video input directly to the HDMI output. A Nios II and the Microtronix Avalon I2C Controller is used to configure the HDMI devices. The Receiver board is preprogrammed with a EDID supporting standard video resolutions. A supplied design also enables the user to reprogram the EDID on the receiver as required to match the desired video resolution of their display monitor.

The Reference Designs are listed in Table 5 below. Additional information is supplied in the Quartus project and on the Installation CD.

**Table 5: Quartus Reference Designs** 

Name / Description	Directory & Filename
HDMI pass-through	example/hsmc_hdmi/: mtx_hdmi.sof
EDID Programming for 60 Hz	example/hsmc_hdmi/: mtx_hdmi_EDID_60.sof
EDID Programming for 50 Hz	example/hsmc_hdmi/: mtx_hdmi_EDID_50.sof

#### **Nios II Source** Code

Source code for the Nios II software be found in can example/hsmc hdmi/software. The two software projects. mtx hdmi bsp and mtx hdmi can be imported into the Nios II IDE with the following procedure.

- 1. Selecting "Import..." from the "File" menu.
- 2. Choose "Altera Nios II" and "Existing Nios II IDE project into workspace" as the import source then click "Next".
- 3. Browse to the mtx hdmi bsp project and click "OK"

- 4. Enter the same project name.
- 5. Click "Finish" to import the project.
- 6. Repeat process for the mtx hdmi project.

## Core

Microtronix I<sup>2</sup>C IP The reference design(s) incorporate the Microtronix I<sup>2</sup>C Master / Slave / PIO Controller IP Core. This core is used in conjunction with an Nios II soft-core processor to initialize and configure the Analog Devices Receiver and Transmitter components and to program EDID EEPROM in the Receiver.

> A 90-day OpenCores Plus licenses is available for testing your custom design in-circuit limited time period before timing out. (Refer to the Altera website for more information.)

> To receive your IP core license contact sales, sales@microtronix.com. and provide them with the serial number of your board and either your NIC or GUARD ID. This license is required for you to recompile and test in-circuit new IP core designs.