Key Features

- 200/333 MHz Cyclone / Stratix memory performance
- SDR, DDR, DDR2 and Mobile DDR SDRAM memory devices
- Up to 10 local bus RD or WR ports
- Configurable FIFO depth: 16 to 2048 bytes
- Memory data width: 8/16/32/64-bit
- Local bus width from 8 to 128-bits
- Intelligent SDRAM burst caching minimizes wait-states
- Layout independent DDR Round-Trip capture scheme
- Multiple time domain clocking
- Configuration GUI streamlines design process
- Supports Cyclone I, II, III, Stratix I, II, II-GX, III

Advanced Performance Architecture

- Source synchronous clocking simplifies DDR timing closure
- Configurable FIFO optimizes streaming video applications
- Configurable memory and local bus data width
- Independent time domain clocking optimizes memory bandwidth
- Round-robin bus arbitration
- SDRAM DQ groups not restricted to dedicated DQ pins.

Target Applications

The core is targeted at applications requiring high-performance memory subsystems including: HDTV consumer electronics, video conversion / enhancement equipment, military vision systems, medical imaging, data networking, Ethernet, PCIe, data recorders.

For example, in consumer products, the core provides the essential building block for developing video and image enhancement systems including; video interlacing, de-interlacing, 720p/1080i/1080p scalers, 100/120 Hz, display systems, image processing, noise filtering or removal of artifacts. For the broadcast industry with the move to HD content, there is a great need to convert standard-definition (SD) content to HD format and for 60/50 and 50/60 Hz refresh rate conversion. This SD content must be de-interlaced and upsampled from 480i to 1080p without introducing fringing, noise or artifacts. Generally the technology solution required by each of these applications will incorporate multiple bus ports interconnected onto a single high-bandwidth SDRAM memory array; a role in which the Microtronix IP core is ideally suited.

Description

The Microtronix Streaming Multi-port SDRAM Memory Controller IP Core integrates: a burst SDRAM memory controller core, a port arbitrator and intelligent look-ahead FIFO controller into one easy-to-use core. By supporting SDR&DDDR/DDR2 and Mobile DDR device families in a single IP Core assures designers of a smooth low-risk migration path with changing technology.

The core supports up to six independently clocked streaming data sources operating from one shared high bandwidth memory system. Using the intuitive Microtronix GUI interface, with a few clicks of a mouse, designers can create a multi-port system, a design task which would normally take several man-months of effort!
Technical Description

One of the key performance features of the Microtronix Streaming Multi-port Memory Controller IP core is a proprietary source-synchronous design technique used for capturing the high-speed DDR data from the memory devices independent of the round-trip delay. The method makes IP core timings independent of the PCB layout trace length signal delay and any associated impedance variance of the board fabrication process. The source-synchronous clocking also frees the IP core design task from the PCB design step and reduces the FPGA design compilation to a simple two-step process!

This proprietary source-synchronous data capture technology also removes the extra resynchronization clocks required by PLL based designs boosting the performance of the memory system by 20%.

Other Features and IP Core Deliverables

• VHDL IP functional simulations models
• On Die Termination (ODT) improves signal integrity
• Includes perpetual license and 1 year of updates
• Altera OpenCore Plus evaluation
• The IP Core can be customized for more system ports.

Memory Timing GUI

This clocking concept also expands data capture timing margins extending temperature performance and enabling faster timing closure in the design fitting process.

Memory Performance (MHz)

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>SPEED GRADE (COMMERCIAL)</th>
<th>SDR SDRAM</th>
<th>DDR SDRAM</th>
<th>DDR2</th>
<th>MOBILE DDR</th>
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<tbody>
<tr>
<td>Arria GX</td>
<td>-6</td>
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<td>200</td>
<td>267</td>
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<tr>
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<td>133, 166</td>
<td>133, 166</td>
<td>133, 166</td>
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<tr>
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<td>180, 200, 200</td>
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<td>160, 180, 200, 166, 166, 166</td>
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Ordering Info

• SKU: 6248-01-01 Streaming Multi-port SDRAM Memory Controller IP Core
• www.microtronix.com